RECEIVED
CENTRAL FAX CENTER
NOV 30 2006

IN THE CLAIMS

1. (Currently Amended) A method for implementing a programmable device, the method comprising:

receiving a high-level language program, the high-level language program configured to run on a conventional central processing unit;

identifying a portion of the high-level language program for hardware acceleration;

generating hardware acceleration logic for performing the portion of the high-level language program on the programmable device, wherein generating hardware acceleration logic comprises identifying pointer access in the portion of the high-level language program; and

coupling the hardware acceleration logic to memory.

2. (Original) The method of claim 1, wherein generating hardware acceleration logic includes generating HDL.

3. (Original) The method of claim 2, wherein generating hardware acceleration logic includes generating a hardware acceleration component for implementation on the programmable device.

4. (Canceled)

5. (Currently Amended) The method of claim 1,~~claim 4,~~ wherein generating hardware acceleration logic includes generating a hardware acceleration component for implementation on the programmable device.

6. (Original) The method of claim 5, providing the hardware acceleration with a write port for a pointer write access identified in the portion of the high–level language program.

7. (Original) The method of claim 6, wherein the write port includes a write address line having an address corresponding to the address of the pointer.

8. (Original) The method of claim 5, providing the hardware acceleration with a read port for a pointer read access identified in the portion of the high–level language program.

9. (Original) The method of claim 6, wherein the read port includes a read address line having an address corresponding to the address of the pointer.

10. (Original) The method of claim 5, wherein the hardware acceleration component is coupled to a simultaneous multiple primary component fabric.

11. (Original) The method of claim 1, wherein the central processing unit is a general purpose processor.

12. (Original) The method of claim 11, wherein the central processing unit supports a general purpose instruction set.

13. (Original) The method of claim 11, wherein the high-level language program is prepared in ANSI C.

14. (Previously Presented) The method of claim 11, further comprising providing a processor core operable as a conventional central processing unit, the processor core configured for implementation on the programmable device.

15. (Original) The method of claim 1, wherein the portion includes multiple disconnected sections of the high-level language program.

16. (Original) The method of claim 1, wherein the portion is identified automatically during parsing of the high-level language program.

17. (Original) The method of claim 1, wherein the portion is identified automatically using profiling data.

18. (Original) The method of claim 17, wherein the profiling data is provided by a profiling and feedback tool.

19. (Original) The method of claim 17, wherein the profiling and feedback tool identifies an optimal hardware acceleration portion.

20. (Currently Amended) A system for implementing a programmable device, the system comprising:

an interface operable to receive a high-level language program, the high-level language program configured to run on a conventional central processing unit;

a processor operable to identify a portion of the high-level language program for hardware acceleration and generate hardware acceleration logic for performing the portion of the high-level language program on the programmable device, wherein generating hardware acceleration logic comprises identifying pointer access in the portion of the high-level language program.

21. (Original) The system of claim 20, wherein the processor is further configured to couple the hardware acceleration logic to memory.

22. (Original) The system of claim 20, wherein generating hardware acceleration logic includes generating HDL.

23. (Original) The system of claim 22, wherein generating hardware acceleration logic includes generating a hardware acceleration component for implementation on the programmable device.

24. (Canceled)

25. (Original) The system of claim 20,~~claim 24,~~ wherein generating hardware acceleration logic includes generating a hardware acceleration component for implementation on the programmable device.

26. (Original) The system of claim 25, providing the hardware acceleration with a write port for a pointer write access identified in the portion of the high–level language program.

27. (Original) The system of claim 26, wherein the write port includes a write address line having an address corresponding to the address of the pointer.

28. (Original) The system of claim 25, providing the hardware acceleration with a read port for a pointer read access identified in the portion of the high–level language program.

29. (Original) The system of claim 26, wherein the read port includes a read address line having an address corresponding to the address of the pointer.

30. (Currently Amended) A system for implementing a programmable device, the system comprising:

means for receiving a high-level language program, the high-level language program configured to run on a conventional central processing unit;

means for identifying a portion of the high-level language program for hardware acceleration;

means for generating hardware acceleration logic for performing the portion of the high-level language program on the programmable device, wherein means for generating hardware acceleration logic comprises means for identifying pointer access in the portion of the high-level language program; and

means for coupling the hardware acceleration logic to memory.

31. (New) A method for implementing a programmable device, the method comprising:

receiving a high-level language program, the high-level language program configured to run on a conventional central processing unit;

identifying a portion of the high-level language program for hardware acceleration, wherein the portion is identified automatically using profiling data;

generating hardware acceleration logic for performing the portion of the high-level language program on the programmable device; and

coupling the hardware acceleration logic to memory.